<u>Rejections to the Drawings</u>

The Examiner stated that the drawings must show every feature of the invention specified in the claims. Therefore, the drawings have been amended to illustrate that the reduced voltage signal is provided to a display (e.g., claim 10). The applicant respectfully submits that no new matter has been added.

<u>Rejections under 35 USC § 102</u>

Claims 1-3, 7, 9, 10, 12-16 stand rejected under 35 USC § 102 as being anticipated by Casper (U.S. Patent No. 5,644,215). The examiner states:

> Regarding claims 1, 12-16, Casper discloses a device comprising an input port (Vcc) to receive the electrical signal from an external sampling point; conditioning circuit, wherein the conditioning circuit comprises (Figure 2) a voltage reducing circuit having output terminals (38) to output a reduced voltage; and a voltage limiting circuit (22) in parallel with the output terminals (38) to limit a voltage across the output terminals when a circuit element within the voltage reducing circuit fails; and a first electrical pathway (through element 22) to electrically coupe the receive electrical signal to the conditioning circuit.
>
> Regarding claim 2, Casper discloses a first resistance; and a second resistance (Resistance after 282) in series with the first resistance, wherein output terminals (38, 30n-i) are across the second resistance.
>
> Regarding claim 3, Casper discloses the voltage limiting circuit (22) comprises transorb.
>
> Regarding claim 7, Casper discloses the reduced voltage signal is provided to a data acquisition system (26).
>
> Regarding claim 9, Casper discloses plurality voltage conditioning circuit is coupled to a circuit under test (18).
>
> Regarding claim 10, Casper discloses the graph (Figure 5-6) displaying the reduced voltage.

Applicant respectfully submits that Casper provides the regulatory circuit described in association with Figure 2. This circuit contains a clamping circuit 22 that "prevents the voltage

between terminals 32 and 34 from exceeding a predetermined clamp value. That is, the clamp circuit 22 limits the voltage between terminals 32 and 34 to the predetermined clamp value." (Casper, Col. 4, lines 17-19.) This regulator circuit is intended to allow an internal voltage to be used in turn provide an activate or deactivate signal to a charge pump.

Applicant respectfully submits that Casper is designed to give a digital output for the detector such that a charge pump is activated or deactivated only when the generator voltage is within a predetermined range.

Applicant's invention provides an interface module for a high voltage circuit in order to condition an electrical signal locally for sampling purposes. Applicant further submits that the clamping circuit shown in Figure 2 of Casper straddles a portion of the voltage divider circuit. No output terminals are provided that in parallel to the clamping circuit and the detector does not sample across the clamping circuit. Rather, threshold detector 26 detects a voltage 36 at some point within the clamping circuit. Neither terminals 32 or 34 of clamping circuit 22 are sampled by detector 26. Further, no reference point is provided from which the output voltage is measured.

With the respect to the examiner's assertion regarding Claim 2, Applicant respectfully submits that although Casper discloses a voltage dividing circuit 24, wherein a portion of the voltage dividing circuit is in parallel with a the clamping circuit, no voltages are detected across the clamping circuit. Applicant respectfully submits that the clamping circuit 22 located across a portion of voltage dividing circuit 24 does not supply an output voltage in parallel with the clamping circuit. Since a voltage limiting circuit is not provided in parallel with the input of the detector circuit and ground (or other reference point), protection is not afforded if any element such as resistive load 28 fail open or short circuit. For example, should resistive load 28_n fail as an open circuit, the detector voltage 36 will approach V_{cc} dependent on the current drawn by the detector. Clamping circuit 22 will have little or no effect on voltage 36. Similarly, should resistive load 28_1 fail as an open circuit, the detector voltage 36 will approach V_{int}. Should these resistive loads fail as short circuits again the sensed voltage would approach V_{int} or V_{cc}. By reducing the potential number of failures by reducing the number of resistive loads, the present invention is able to insure any failure of any resistive load in the voltage reducing network will result in a predetermined safe voltage across the output terminals or that the output terminals are shunted to ground.

Further, the relationship of the resistances in the claimed invention will result in a scaled representation of the input high voltage within a safe predetermined voltage range. This is not afforded by the clamping circuit and voltage dividing circuit taught in Casper.

Applicantrespectfully reverses the examiner's assertion that Casper discloses a transorb for the voltage limiting circuit 22. Applicant notes that transorb is not even contained within the detailed description of Casper.

Regarding Claim 7, Applicant respectfully traverses the examiner's assertion that Casper discloses the reduced voltage signal provided to data acquisition system. Rather, a threshold detector or switch is provided as shown in Figure 2 of Casper.

As Casper fails to teach the invention within Claims 1-3, 7, 9, 10, 12-16, Applicants respectfully request the Examiner withdraw the rejections under 35 USC § 102(b) as being anticipated by Casper and allow Claims 1-3, 7, 9, 10, 12-16.

Claims 1-3, and 12-16 stand rejected under 35 USC § 102(b) as being anticipated by Konrad (U.S. Patent No. 4,835,462). The examiner states:

> Regarding claims 1, 12-16, Konrad discloses a device comprising an input port (16a) to receive the electrical signal from an external sampling point; conditioning circuit (22), wherein the conditioning circuit comprises a voltage reducing circuit (24, 26) having output terminals (Between 24 and 26 and ground) to output a reduced voltage; and a voltage limiting circuit (28) in parallel with the output terminals to limit a voltage across the output terminals when a circuit element within the voltage reducing circuit fails; and a first electrical pathway (through element 28) to electrically coupe the receive electrical signal to the conditioning circuit.
>
> Regarding claim 2, Konrad discloses a first resistance (24); and a second resistance (26) in series with the first resistance (24), wherein output terminals are across the second resistance (26).
>
> Regarding claim 3, Konrad discloses the voltage limiting circuit (28) comprises transorb.

Applicant respectfully submits that Konrad merely limits the voltages observed across R2 with a voltage limited diode 28. No protection is afforded as in provided in the present invention across the output terminals should the voltage dividing circuit fail. Furthermore, applicant respectfully submits that Konrad failed to teach that test equipment may be attached across a resistor such as resistor 26 within the voltage dividing network. Furthermore, Konrad fails to teach that the output terminal are shunted to ground across resistor 26, should resistor 26 fail open by the action of a diode such as diode 48 as shown in Figure 2 of the instant application.

Regarding Claim 2, Applicant submits that no output terminals are shown across resistor 26 as illustrated in Figure 1. With respect to Claim 3, Applicant respectfully submits that Konrad does not mention that the voltage limiting circuit 28 which is shown to be a single diode then comprises a transorb. Transorb is not mentioned within the specifications.

Rejections under 35 USC § 103

Applicant respectfully points out that in order to combine references for an obviousness rejection, there must be some teaching, suggestion or incentives supporting the combination. *In re Laskowski*, 871 F.2d 115, 117, 10 U.S.P.Q. 2d 1397, 1399 (Fed. Cir. 1989). The mere fact that the prior art could be modified does not make that modification obvious unless the prior art suggests the desirability of the modification. *In re Gordon*, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984). In addition, it is well established that Applicant's disclosure cannot be used to reconstruct Applicant's invention from individual pieces found in separate, isolated references. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988).

Claim 4 stands rejected under 35 USC § 103(a) as being unpatentable over Casper (U.S. Patent No. 5,644,215) in view of Rodgers (U.S. Patent No. 4,698,740). The examiner states:

> Regarding claim 4, Casper does not disclose diodes connected in parallel with polarity are reversed.
>
> Rodgers et al. discloses a regulated voltage supply and further discloses (figure 7) a first diode (826) aligned such that if a voltage across terminals (across 825) exceeds a breakdown voltage, the output terminals are shunted reference point (816); a second diode in parallel to the first diode but aligned such that

forward current flow in the second diode is opposite that of diode (See element 826) for the purpose of shunting the converter (Column 2, lines 50-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the diodes configured in parallel as taught by Rodgers et al. into the system of Casper because using diodes connected in parallel with polarity reversed is routine for the purpose of shunting.

Applicant respectfully submits that there is no motivation, teaching or suggestion to combine Casper with Rodgers. Therefore, the rejection on a combination of these references is inappropriate. Withdrawal of the rejection allowance of Claim 4 is respectfully requested.

In addition to the previous arguments regarding Casper, Applicant further submits that neither Casper or Rodgers alone nor the combination of the two teaches or suggests make obvious the invention recited in Claim 4 because the cited reference do not disclose diodes connected in parallel with polarity are reversed. Rodgers discloses that element 826 is a triac. A triac is a three terminal semiconductor for controlling current in either direction. The schematic symbol for the triac looks like two SCRs in parallel (opposite direction) with one trigger or gate terminal. No gate is provided in the instant application as two diodes are present.

Applicant, therefore, respectfully requests the Examiner to reconsider and withdraw the rejection to allow Claim 4.

Claims 5, 6, 11, stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casper (5,644,215). The examiner states:

Regarding claims 5, 6, Casper does not disclose the ratio of the second resistance to the sum of first resistance is about 1/101.01.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the ratio of the second resistance to the sum of first resistance is about 1/101.01 and the reduced voltage does not exceed 40 voltages into the system of Casper, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ215 (CCPA 1980).

Regarding claim 11, Casper does not disclose a first failure in either first or second resistance does not result in a reduced voltage exceeding a predetermined safe voltage. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the resistance values in a series configuration and shunting diodes so that a failure in either first or second resistance does not result in a reduced voltage exceeding a predetermined safe voltage because selecting the values for the resistance R2 in the voltage divider R2/ (R1+R2) is principle of Ohm law.

Applicant respectfully traverses the examiners arguments and respectfully submits that as amended the present invention addresses samples a high voltage and applies a voltage divider having output terminals across a resistive element and voltage limiting circuit in order to limit the actual voltage sensed by external test equipment sampling the output terminals to a predetermined voltage. While electrical circuits may operate under the principle of Ohm's law, the applicant respectfully submits that Ohm's law did not teach or make obvious the claimed invention.

Applicant, therefore, respectfully requests the Examiner to reconsider and withdraw the rejection to allow Claims 5, 6 and 11.

Claims 8, 17, 18, stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casper (5,644,215) in view of Weberg (4,099,216). The examiner states:

Regarding claims 8, 17, Pertinence to the discussion of claim 1 above, Casper does not disclose an epoxy package encapsulates the conditioning circuit.

Weberg discloses a fuseless intrinsic safety barrier and further discloses an epoxy package (figure 1) encapsulates the conditioning circuit (10) for the purpose of enhancing the safety (Column 2, lines 44-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the epoxy package encapsulates the conditioning circuit as taught by Weberg into the system of Casper because insulating the circuit would have been desirable for the safety.

Regarding claim 18, Casper discloses the voltage limiting circuit comprises a transorb (22).

Applicant respectfully submits that there is no motivation, teaching or suggestion to combine Casper with Weberg. In addition to the previous arguments regarding Casper, Applicant further submits that neither Casper nor Weberg alone nor the combination of the two teaches or suggests make obvious the invention recited in Claims 8, 17 and 18. Therefore, the rejection on a combination of these references is inappropriate. Casper fails to teach the application of a voltage divider and voltage limiting circuit as taught in the claimed invention for the reasons stated above. Encasing the claimed invention within epoxy to enhance electrical safety is not taught within Weberg. Weberg teaches that the epoxy may be used as a barrier to unsafe atmospheres. (Weberg, Col. 2, lines 44-53) Furthermore, Weberg does not provide a circuit one would couple to data acquisition equipment. Therefore one would not apply the teachings of Weberg to the claimed invention. Applicant, therefore, respectfully requests the Examiner to reconsider and withdraw the rejection to allow Claim Claims 8, 17 and 18.

Claims 19-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Casper (5,644,215) in view of Weberg (4,099,216), as applied to claim 17 above, and further in view of in view of Rodgers et al. (4,698,740). The examiner states:

> Regarding claim 19, Casper and Weberg do net disclose diodes connected in parallel with polarity are reversed.
>
> Rodgers et al. discloses a regulated voltage supply and further discloses (figure 7) a first diode (826) aligned such that if a voltage across terminals (across 825) exceeds a breakdown voltage, the output terminals are shunted reference point (816); a second diode in parallel to the first diode but aligned such that forward current flow in the second diode is opposite that of diode (See element 826) for the purpose of shunting the converter (Column 2, lines 50-56).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the diodes configured in parallel as taught by Rodgers et al. into the system of Casper because using diodes connected in parallel with polarity reversed is routine for the purpose of shunting.
>
> Regarding claims 20, 21, Casper does not disclose the ratio of the second resistance to the sum of first resistance is about 1/101.01.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the ratio of the second resistance to the sum of first resistance is about 1/101.01 and the reduced voltage does not exceed 40 voltages into the system of Casper, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ215 (CCPA 1980).

Regarding claim 22, Casper discloses the reduced voltage signal is provided to a data acquisition system (26). Regarding claim 23, Casper discloses the graph (Figure 5-6) displaying the reduced voltage.

Regarding claim 24, Casper does not disclose a first failure in either first or second resistance does not result in a reduced voltage exceeding a predetermined safe voltage.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the resistance values in a series configuration and shunting diodes so that a failure in either first or second resistance does not result in a reduced voltage exceeding a predetermined safe voltage because selecting the values for the resistance R2 in the voltage divider R2/ (Ri+R2) is principle of Ohm law.

Applicant respectfully submits that there is no motivation, teaching or suggestion to combine Casper with Weberg and Rodgers. Therefore, the rejection on a combination of these references is inappropriate. Withdrawal of the rejection allowance of Claims 19-24 is respectfully requested.

In addition to the previous arguments regarding Casper, Weberg and Rodgers, Applicant further submits that neither alone nor the combination of these references teaches, suggests or make obvious the invention recited in Claims 19-24. These references either alone or in combination fail to teach the claimed invention. The applicant respectfully traverses the examiners arguments and respectfully submits that as amended the present invention addresses samples a high voltage and applies a voltage divider having output terminals across a resistive element and voltage limiting circuit in order to limit the actual voltage sensed by external test equipment sampling the output terminals to a predetermined voltage. The cited reference fail to teach that a voltage sensing or test

equipment be applied across the terminals of a voltage limiting circuit in parallel with a portion of a voltage divider.

Applicant, therefore, respectfully requests the Examiner to reconsider and withdraw the rejection to allow Claim Claims 19-24.

REMARKS

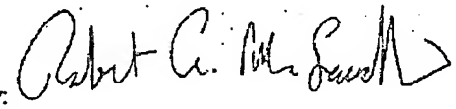
Applicants appreciate the time taken by the Examiner to review Applicants' present application. This application has been carefully reviewed in light of the Official Action mailed November 24, 2004. Applicants respectfully request reconsideration and favorable action in this case.

CONCLUSION

Applicants have now made an earnest attempt to place this case in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-24.

While Applicants believe no fee is due with this transmission, if any fees are due, the Commissioner is hereby authorized to charge Deposit Account No. 50-2240 of Koestner Bertani.

Respectfully submitted,

By: 

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